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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,372	07/31/2001	Vadim Gutnik	5347-205	2525
20792 7590 11/30/2005		EXAMINER		
MYERS BIGEL SIBLEY & SAJOVEC			CHUNG, PHUNG M	
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RALEIGH, NC 27627			ART UNIT	PAPER NUMBER
			2138	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)		
Office Action Summary		09/919,372	GUTNIK ET AL.		
		Examiner	Art Unit		
		Phung My Chung	2138		
Period fo	The MAILING DATE of this communication app or Reply	pears on the cover sheet with the	correspondence address		
A SH WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING Donsions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. Depended for reply is specified above, the maximum statutory period vire to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be will apply and will expire SIX (6) MONTHS from the course the application to become ABANDON	ON. timely filed om the mailing date of this communication. NED (35 U.S.C. § 133).		
Status					
1)🛛	Responsive to communication(s) filed on <u>02 S</u>				
2a)∐	,—				
3)	closed in accordance with the practice under <i>E</i>	·			
	·	Ex parte Quayre, 1905 C.D. 11,	+55 O.G. 215.		
Disposit	ion of Claims				
5)⊠ 6)⊠ 7)□	Claim(s) <u>1-26</u> is/are pending in the application 4a) Of the above claim(s) is/are withdraw Claim(s) <u>8-13</u> is/are allowed.  Claim(s) <u>1-7 and 14-26</u> is/are rejected.  Claim(s) is/are objected to.  Claim(s) are subject to restriction and/o	wn from consideration.			
Applicati	ion Papers				
10)	The specification is objected to by the Examine The drawing(s) filed on is/are: a) acc Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Examine	epted or b) objected to by the drawing(s) be held in abeyance. Stion is required if the drawing(s) is c	See 37 CFR 1.85(a). Objected to. See 37 CFR 1.121(d).		
Priority ι	ınder 35 U.S.C. § 119		•		
12)☐ a)l	Acknowledgment is made of a claim for foreign All b) Some * c) None of:  1. Certified copies of the priority document:  2. Certified copies of the priority document:  3. Copies of the certified copies of the priority application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in Applica rity documents have been recei u (PCT Rule 17.2(a)).	ation No ved in this National Stage		
Attachmen	<b>t(s)</b> e of References Cited (PTO-892)	<b>0</b> □ · · •	v. (DTO 442)		
2) 🔲 Notic 3) 🔲 Inforr	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date	4)  Interview Summa Paper No(s)/Mail 5)  Notice of Informal 6)  Other:			

1. Claims 1-7 and 14-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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As per claim 1, lines 2-3, "a first clock circuit... generate a first clock signal responsive to an error signal" is unclear because there must be an error detecting circuit for detecting error appeared before introducing an error signal, what kind of error signal is that? and how the error signal is detected?

Lines 6-8, "a phase detector... to generate the error signal responsive to the first and second clock signals" is not clear whether the error signal is the same error signal that introduced in line 3 or not.

As per claim 2, lines 4-5, "a third clock circuit... to generate a third clock signal responsive to a second error signal" is not clear how the second error signal is detected; and lines 6-8, "a second phase detector circuit... to generate the second error signal... signals" is not clear whether the second error signal is the same as the error signal that introduced in line 5.

As per claims 3-7, these claims are also rejected because they dependent upon the rejected base claims.

As per claims 14-15 and 19-20, these claims are rejected under similar rationale as set forth in claims 1-2.

As per claims 16-18 and 21-24, these claims are also rejected because they dependent upon the rejected base claims.

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2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doblar et al (6,516,422) in view of Oshio (6,510,013).

As per claim 26, Doblar et al disclose an apparatus, comprising:

A means for independently generating a plurality of clock signals on an integrated circuit; and

A phase detector is configured to produce a phase error signal indicative of the different between the clock signals (col. 4, lines 18-24 and col. 6, lines 18-23). Doblar et al do not disclose a means for synchronizing phases of the plurality of clock signals to one another based on error signals that are generated based on relative phase difference between ones of the plurality of clock signals. However, Oshio discloses a

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means for synchronizing phases of clock signals with one another (col. 4, lines 59-67 to col. 5, lines 1-4). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the means for synchronizing phases of clock error signals as taught by Oshio into the invention of Doblar et al to adjust the timing or phase of the phase synchronizing signal such that the detected phase-error is nullified.

As per claim 25, this method claim is rejected under similar rationale as set forth in the system claim 26.

- 4. Claims 8-13 are allowable.
- 5. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.
- 6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung

Primary Patent Examiner

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